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High-Performance Nonvolatile Organic Transistor Memory Devices Using the Electrets of Semiconducting Blends

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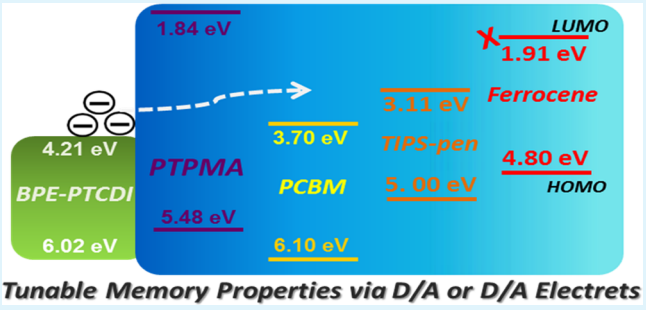
Supporting Information

ABSTRACT: Organic nonvolatile transistor memory devices of the *n*-type semiconductor *N*,*N*′-bis(2-phenylethyl)-perylene-3,4:9,10-tetracarboxylic diimide (BPE-PTCDI) were prepared using various electrets (i.e., three-armed star-shaped poly[4-(diphenylamino)benzyl methacrylate] ($N(PTPMA)_3$) and its blends with 6,6-phenyl-C_{61}-butyric acid methyl ester (PCBM), 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pen) or ferrocene). In the device using the PCBM:$N(PTPMA)_3$ blend electret, it changed its memory feature from a write-once-read-many (WORM) type to a flash type as the PCBM content increased and could be operated repeatedly based on a tunneling process. The large shifts on the reversible transfer curves and the hysteresis after implementing a gate bias indicated the considerable charge storage in the electret layer. On the other hand, the memory characteristics showed a flash type and a WORM characteristic, respectively, using the donor/donor electrets TIPS-pen:$N(PTPMA)_3$ and ferrocene:$N(PTPMA)_3$. The variation on the memory characteristics was attributed to the difference of energy barrier at the interface when different types of electret materials were employed. All the studied memory devices exhibited a long retention over 10^4 s with a highly stable read-out current. In addition, the afore-discussed memory devices by inserting another electret layer of poly(methacrylic acid) (PMAA) between the BPE-PTCDI layer and the semiconducting blend layer enhanced the write-read-erase-read (WRER) operation cycle as high as 200 times. This study suggested that the energy level and charge transfer in the blend electret had a significant effect on tuning the characteristics of nonvolatile transistor memory devices.



KEYWORDS: *transistor, nonvolatile memory, polymer electret, charge-storage layer, donor−acceptor, energy level*

1. INTRODUCTION

Organic semiconductors have attracted extensive research interest in electronic devices, such as transistors, photovoltaics, and memories, due to the advantages of the low-cost fabrication, mechanical flexibility, and ease of processing. Among the organic memory devices,[1−8] the devices using field-effect transistor (FET) device structures are considered to be one of the emerging technologies for developing high density data storage devices.[9−14] Effectively controlling the threshold voltage shifts on the transfer curves in FET memory devices has been achieved using an additional charge-trapping layer, such as ferroelectric materials,[15−17] nanofloating gate dielectrics,[18−23] and polymer-based electrets.[24−30]

The FET memory devices using polymer-based electrets could sustain low-cost fabrication processes without the demand of metallic nanoparticles or ferroelectric materials.[24−30]

The high-polar hydroxyl-containing polymers including poly(4-vinylphenol) (PVP) and poly(vinyl alcohol) (PVA)[21,30−32] were demonstrated to have the capacity of trapping mobile electrons but suffered from the relatively poor retention characteristics due to the dissipation of an electric-field induced dipole. We previously developed the electrets with high electron-trapping ability via incoporation of conjugated moieties into polymer side chains to obtain the flash and write-once-read-many (WORM) memory characteristics based on the difference in energy levels between the active layer and electrets.[25−27]

In addition, a further enhancement of the memory window can be realized by blending the polymer layer with well-known semiconducting molecules.[33−36] Wu et al. revealed that the copper phthalocyannine (CuPc)-based memory device using the poly(methyl methacrylate)/electron-donating molecules (such as tetrathiafulvalene, or ferrocene) blend electrets showed the flanks of the hysteresis and a retention longer than 24 h.[33] We recently reported a low-voltage-operating nonvolatile organic field-effect transistor (OFET) memory with a reliable

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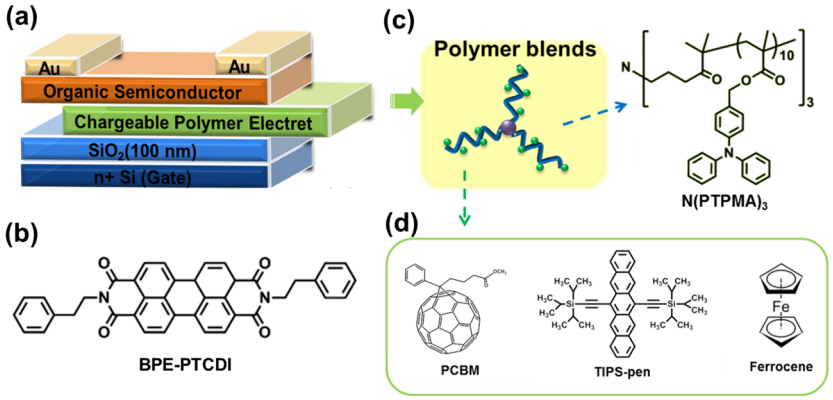

Figure 1. (a) Schematic configuration of the OFET memory device and (b) the chemical structure of *n*-type BPE-PTCDI active layer. (c) Polymer dielectric of $N(PTPMA)_3$ and (d) organic materials of PCBM, TIPS-pen, and ferrocene, used in the blend electret.

bending stability using the high-k poly(methacrylic acid) blended with graphene oxide electret.[36] On the other hand, [6,6]-phenyl-C_{61}-butyric acid methyl ester (PCBM) employed in gate dielectric for a *p*-type transistor provided the electric-field induced charge transfer that led to a hysteresis loop with a threshold voltage shift.[34,37] However, the tuning on the FET memory characteristics through the charge transfer of the donor−donor or donor−acceptor blend electrtes have not been fully explored yet.

Here, we explored the organic nonvolatile transistor-type memory characteristics using the active layer of the *n*-type semiconductor, *N*,*N*′-bis(2-phenylethyl)-perylene-3,4:9,10-tetracarboxylic diimide (BPE-PTCDI), and the blend electrets composed of three-armed star-shaped poly[4-(diphenylamino)-benzyl methacrylate] ($N(PTPMA)_3$) and various semiconducting materials (i.e., PCBM, 6,13-bis(triisopropylsilylethynyl)-pentacene (TIPS-pen), and ferrocene), as shown in Figure 1. The OFET memory devices were fabricated using a bottom-gate/top-contact structure (Figure 1a). The charge-trapping and memory characteristics using the donor/donor and donor−acceptor blend electrets were studied. In addition, the operational mechanism of memory-switching properties in terms of an energy-band diagram was investigated. Our experimental results provide a systematic study on establishing the relationship between the memory characteristics and the electroactive blend composition.

2. EXPERIMENTAL SECTION

2.1. Materials. The three-armed star-shaped poly[4-(diphenylamino)benzyl methacrylate] ($N(PTPMA)_3$; M_n = 6.2 kg mol^{-1}, M_w/M_n = 1.10) was synthesized via organocatalyzed group transfer polymerization as reported previously.[38] *N*,*N*′-Bis(2-phenylethyl)perylene-3,4,9,10-bis(dicarboximide) (BPE-PTCDI) and [6,6]-phenyl-C_{61}-butyric acid methyl ester (PCBM) were purchased from Luminescence Technology Corp (Taiwan) and Nano-C Inc., respectively. Poly(methyl methacrylate) (PMMA; M_w ∼ 350 kg mol^{-1}), ferrocene, and 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pen) were purchased from Sigma-Aldrich (Missouri, USA). Poly(methacrylic acid) (PMAA) was obtained from Scientific Polymer Products Inc. All anhydrous solvents were commercially available and used as received.

2.2. Device Fabrication. As shown in Figure 1a, the OFET memory device was fabricated with a top-contact configuration on a highly doped *n*-type Si substrate with a thermally grown 100 nm thick SiO_2 dielectric. The substrate was rinsed with toluene, acetone, and isopropyl alcohol and then dried with a stream of nitrogen before use. A toluene solution of $N(PTPMA)_3$ (10 mg mL^{-1}) containing a calculated amount of PCBM was stirred overnight to afford a homogeneous solution. Thereafter, the solution was filtered through a PTFE membrane syringe filter (pore size, 0.22 μm) and deposited onto the SiO_2 layer by spin-coating at 1000 rpm for 60 s. The polymer films were dried at 70 °C for 1 h under vacuum (10^{-6} Torr) to remove residual solvents and estimated to have a thickness of ca. 50 nm. The semiconducting BPE-PTCDI thin films (50 nm) were thermally deposited at an evaporating rate of 0.5 Å s^{-1} under about 10^{-7} Torr with the maintenance of substrate temperature at 90 °C. Then 100 nm

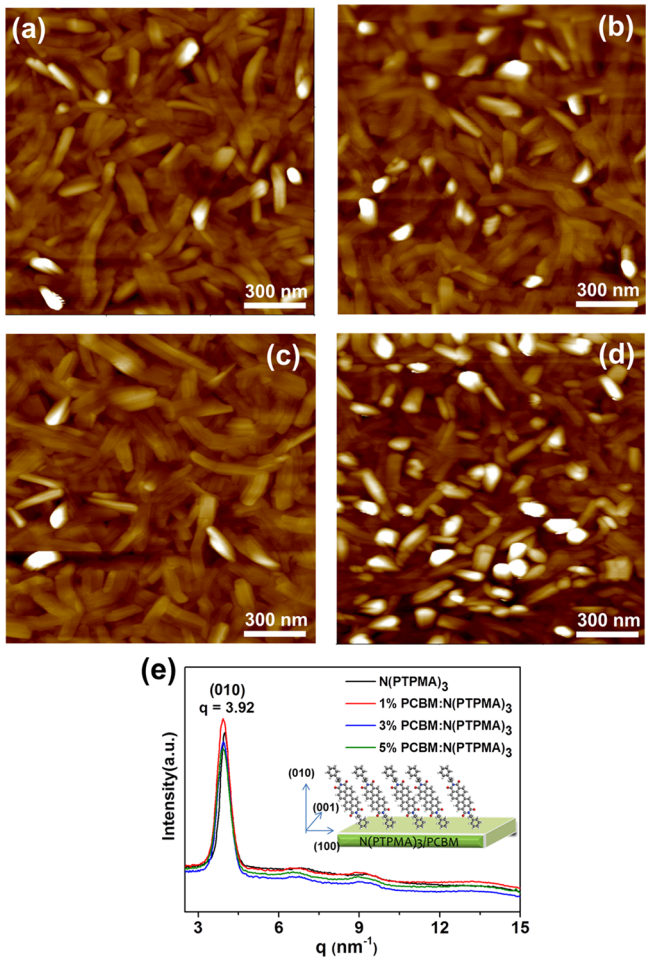

Figure 2. AFM topographies of BPE-PTCDI film deposited on (a) $N(PTPMA)_3$, (b) 1 wt % PCBM:$N(PTPMA)_3$, (c) 3 wt % PCBM:$N(PTPMA)_3$, and (d) 5 wt % PCBM:$N(PTPMA)_3$. (e) X-ray diffraction patterns of the 50 nm thick BPE-PTCDI films deposited on different dielectric surfaces.

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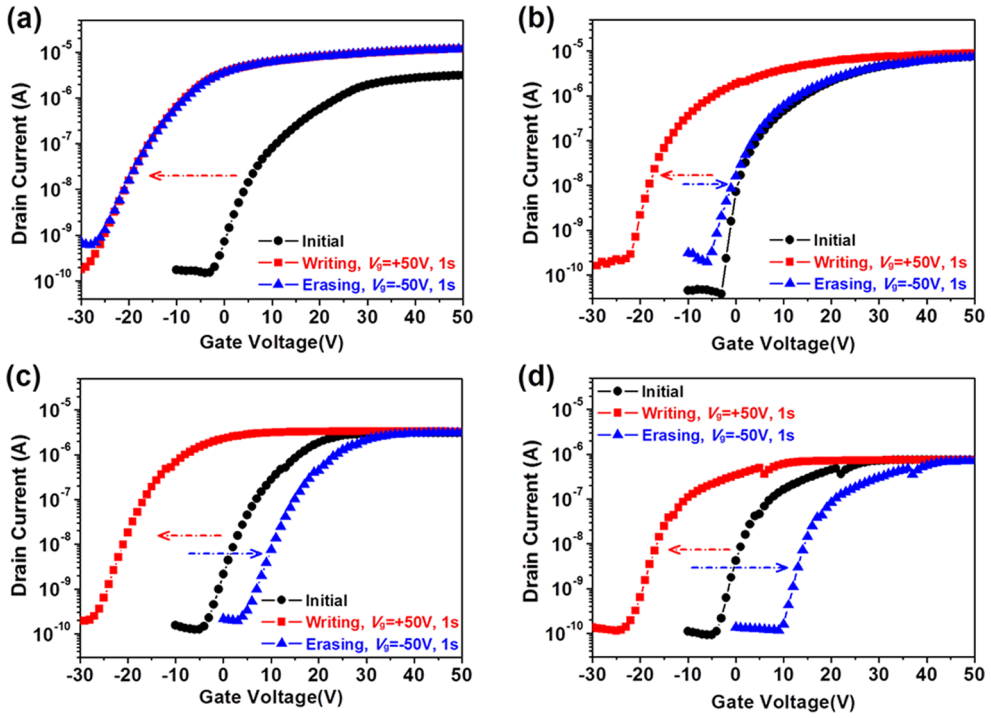

Figure 3. Transfer curves of transistor memory devices with (a) $N(PTPMA)_3$, (b) 1 wt % PCBM:$N(PTPMA)_3$, (c) 3 wt % PCBM:$N(PTPMA)_3$, and (d) 5 wt % PCBM:$N(PTPMA)_3$ as electrets. The drain current was measured at V_{ds} = 30 V.

Table 1. Properties of BPE-PTCDI Transistor Memory with Various Charge Storage Electrets

	μ_{ave} [$cm^2\ V^{-1}\ s^{-1}$]	I_{ON}/I_{OFF}	$V_{th,ave}$ [V]	$V_{th,ave}$ [V] writing	$V_{th,ave}$ [V] erasing	memory window [V]	memory type
$N(PTPMA)_3$	0.0274 ± 0.0007	6.63×10^6	6.14 ± 0.9	−17.86	−17.60	0.26 ± 1.02	WORM
1 wt % PCBM:$N(PTPMA)_3$	0.0215 ± 0.0080	1.97×10^6	0.93 ± 0.5	−14.10	3.79	17.89 ± 6.72	flash
3 wt % PCBM:$N(PTPMA)_3$	0.0247 ± 0.0099	3.09×10^5	3.44 ± 0.2	−22.71	10.84	33.55 ± 2.80	flash
5 wt % PCBM:$N(PTPMA)_3$	0.0050 ± 0.0005	3.25×10^5	−2.81 ± 1.5	−18.26	12.70	30.96 ± 1.72	flash
5 wt % TIPS-pen:$N(PTPMA)_3$	0.0027 ± 0.0007	5.66×10^5	0.31 ± 0.13	−17.73	11.03	27.95 ± 4.24	flash
5 wt % ferrocene:$N(PTPMA)_3$	0.0332 ± 0.0042	6.63×10^6	4.58 ± 1.86	−21.10	−20.29	0.81 ± 0.45	WORM

thick gold electrodes were subsequently deposited by thermal deposition through a shadow mask as source and drain electrodes. The channel length (L) and width (W) of the devices were 50 and 1000 μm, respectively.

Similarly, the $N(PTPMA)_3$:TIPS-pentacene and N-$(PTPMA)_3$:ferrocene blends were dissolved in toluene (10 g L^{-1}) and then deposited onto the SiO_2 layer. The thickness of the TIPS-pentacene:$N(PTPMA)_3$ and ferrocene:$N(PTPMA)_3$ layers were also estimated to be around 50 nm. The process of device fabrication was similar to that of the original device.

2.3. Characterization. The degree of aggregation of PCBM in the $N(PTPMA)_3$:PCBM layer was investigated using transmission electron microscopy (TEM, JEOL 1230) at an acceleration voltage of 100 kV. The samples for TEM measurements were prepared by spin-coating onto a 200 mesh carbon-coated copper grid. The thickness and surface morphologies of the $N(PTPMA)_3$:PCBM layer were analyzed by a Microfigure measuring instrument (Surfacorder ET3000, Kosaka Laboratory Ltd.) and atomic force microscopy (AFM, Nanoscope 3D controller, Digital Instruments, operated in the tapping mode at room temperature (rt)), respectively. The X-ray diffraction (XRD) data were collected using a Mar345 image plate detector with a sample-to-detector distance of 213 mm. The angle of incidence was 0.2°. Data were recorded in the range of q = 0.2 − 15.0 nm^{-1} and collected for 1 min.

The electrical characterization of the memory were carried out using a Keithley 4200-SCS semiconductor parameter analyzer with Remote PreAmp (4200-PA) in a N_2-filled glovebox at rt. Triaxial cables were connected onto the probe station to minimize the background noise. The measurements were carried out in a dark environment to prevent the light-induced charge transfer or excitons.[7,8] The carrier mobility (μ) and threshold voltage (V_{th}) can be estimated from the slope and intercept of the linear plot of the square root of drain-to-source current ($(I_{ds})^{1/2}$) versus the gate voltage (V_g) by the following equation within the saturation regime:

$$I_{ds} = \frac{WC_{tot}\mu}{2L}(V_g - V_{th})^2$$

where C_{tot} is the capacitance per unit area of total dielectric layer and V_{th} is threshold voltage. For the capacitance measurement, a metal−insulator−metal (MIM) structure was fabricated by depositing gold electrodes on the polymer-coated indium tin oxide (ITO) substrate. The capacitance of the bilayer dielectrics was measured on MIM structures using a Keithley 4200-SCS instrument equipped with a digital capacitance meter (model 4210-CVU).

3. RESULTS AND DISCUSSION

3.1. Effect of PCBM:$N(PTPMA)_3$ Blend Ratio on Memory Characteristics. Figure 1 shows a schematic configuration of BPE-PTCDI transistor memories using the PCBM:$N(PTPMA)_3$ electret (PCBM; 0, 1, 3, and 5 wt %, respectively). The AFM images of the electret suggest that each PCBM:$N(PTPMA)_3$ layer has a rather smooth morphology

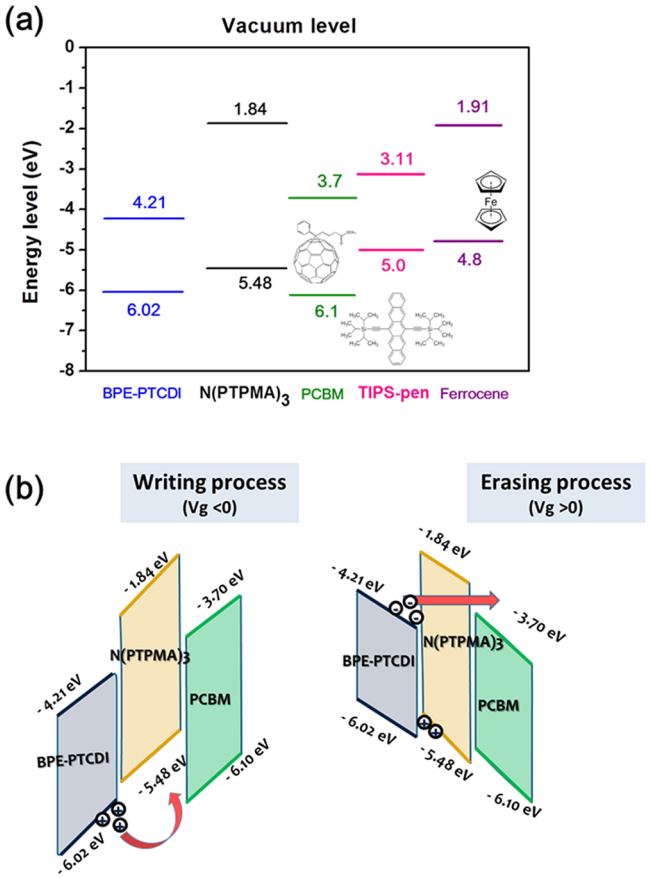

Figure 4. (a) Energy level diagrams of the studied materials and (b) proposed electrical switching mechanism.

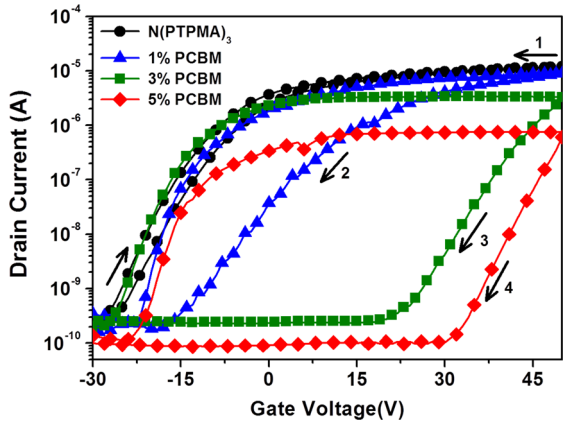

Figure 5. Hysteresis loop measured at V_d = 30 V on the BPE-PTCDI-based TFT memory devices operated in the writing process (V_g = +50 V, 1s).

with roughness below 1 nm, as shown in Figures S1 and S2 (Supporting Information), respectively. The dark spots observed in the TEM images can be attributed to the PCBM aggregates whose sizes are ca. 10 nm and ca. 20 nm in the 3 wt % PCBM:N(PTPMA)$_3$ and 5 wt % PCBM:N(PTPMA)$_3$ composites (Figure S1b,c, Supporting Information), respectively. On the contrary, the 1 wt % PCBM:N(PTPMA)$_3$ layer does not exhibit obvious aggregation (Figure S1a, Supporting Information). It indicates the star-shaped architecture of N(PTPMA)$_3$ and charge transfer between triphenylamine moiety and PCBM limit the PCBM aggregation in the

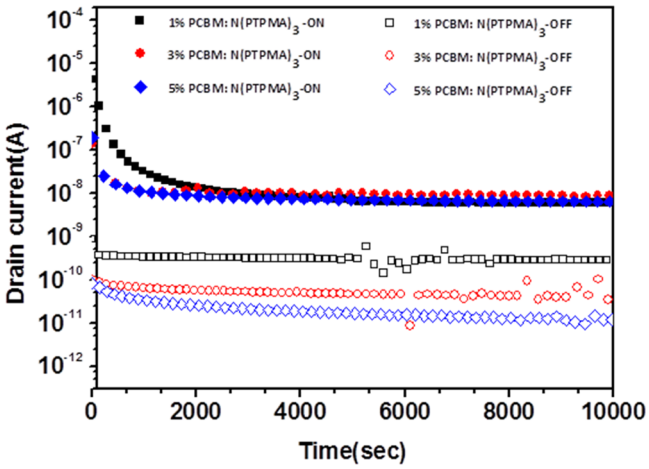

Figure 6. Retention characteristics of BPE-PTCDI-based OFET memory devices with various dielectrics measured at drain-source voltage of 30 V.

composite film.[38] Moreover, it has been known that N-(PTPMA)$_3$ can be used as a passivation layer to improve the crystalline growth of BPE-PTCDI because of its hydrophobic properties.[26] As observed in the AFM images (Figure 2a–d), the vacuum-deposited BPE-PTCDI grows to rod-like crystals on the N(PTPMA)$_3$:PCBM layer with an optimized molecular packing. On the other hand, no significant morphology is shown by adjusting blend compositions. The *d*-spacing of 1.578 nm of the high crystalline BPE-PTCDI films, extracted from the out-of-plane XRD patterns in Figure 2e, is extremely close to that reported in the literature.[39,40] It is observed that the long axis of BPE-PTCDI molecules orients in a parallel direction with the substrate and the plane of π-stacking is parallel to the substrate surface.

The electrical transfer characteristics of the OFET memory devices using the PCBM:N(PTPMA)$_3$ electret are shown in Figure 3. It is clearly observed that these transfer curves exhibit a typical *n*-type accumulation mode. As summarized in Table 1, the mobility (μ) of these devices is in the range of 10^{-2}–10^{-3} cm^2/(V s) and agrees well with the reported values,[40] indicating the high crystalline of BPE-PTCDI. The μ of OFET using the PCBM:N(PTPMA)$_3$ electrets (0.50–2.47 × 10^{-2} cm^2/(V s)), especially for the device with a high-content PCBM (5 wt %), is lower than that using the N(PTPMA)$_3$ electret (2.74 × 10^{-2} cm^2/(V s)) at the source-drain voltage of 30 V. Moreover, the devices using the PCBM:N(PTPMA)$_3$ electrets also show a relatively low saturation drain current, suggesting the PCBM ingredient has a significant effect on the electrical transfer characteristics. It has been widely accepted that the added PCBM can withdraw the mobile negative charges from the conductive channel an electrical-field applies, due to its electron-accepting feature.[34,35,37,41] Notably, the devices afford a high On/Off current ratio of 10^5–10^6 and low threshold voltage (V_{th}), suggesting the potential applications of the fabricated transistor memories.

To switch the conductance of memory devices, the charge-transfer process is investigated by adjusting the electric field through exerting the pulse of the gate voltage. When the negative gate bias (V_g = −50 V, 1 s) is applied, the negative shift is observed and considered to be induced by the hole injection from the semiconductor layer into the dielectric layer. This negative shift is referred to as the writing process. On the

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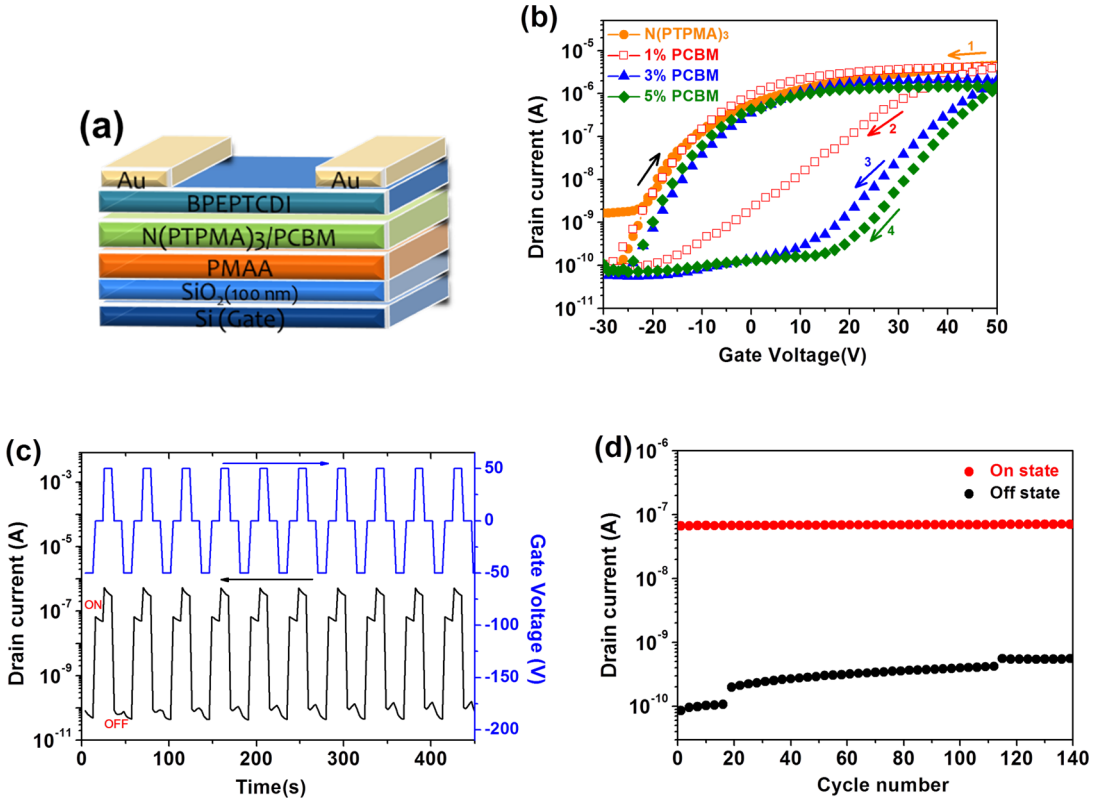

Figure 7. (a) Modified structures of the studied OFET memory. (b) Hysteresis loop of BPE-PTCDI-based TFT memories after inserting PMAA during the writing process. (c) Switching behavior for BPE-PTCDI-based memory device with 5 wt % PCBM:N(PTPMA)$_3$/PMAA bilayer electret, and (d) record of ON and OFF current of 140 cycles for the switching behavior.

other hand, the opposite pulse of gate voltage (V_g = 50 V, 1s) would induce the electron injection into the dielectric and lead to the positive shift, referred to as the erasing process. For the BPE-PTCDI-based OFET device without the electret layer (Figure S3, Supporting Information), it has a negligible memory window (<5 V) and does not show an obvious trapping effect, suggesting that no charges are trapped by impurity centers and structural defects within the semiconductor layer. On the basis of the above results, it is also rational to assume that, after implementing the pulse of gate voltage, the substantial V_{th} shifts in the transistor memory device originated from the additional PCBM:N(PTPMA)$_3$ dielectric layer.

Defined by the V_{th} shift between the writing and erasing process, the memory windows obtained from the transfer characteristics (Figure S4, Supporting Information) are summarized in Table 1. In the device only using the N(PTPMA)$_3$ electret, the large V_{th} shift in the writing curve is observed but nonerasable, indicating that this device is a write-once-read-many-times (WORM) type memory. Thus, the current cannot recover to the initial state once it switches to the high conductance state (Figure S5, Supporting Information). The above irreversible behavior is considered to be originated from the strong electron-donating nature of the pendent triphenylamine moieties in the polymer side chains.[26] In comparison, as the PCBM is blended into N(PTPMA)$_3$, the memory nature of the device switches to be a nonvolatile flash type and becomes erasable because the blending of PCBM into N(PTPMA)$_3$ enables the negative charge to be stored in the dielectric layer. As shown in Figure 3b–d, under the erasing process, the shifts toward the positive region in the transfer curves are 3.79, 10.84, and 12.70 V when PCBM is blended at weight ratios of 1, 3, and 5 wt %, respectively. In addition, a large memory window (~33.55 V) is observed in the device using the 3 wt % PCBM:N(PTPMA)$_3$ electret. It has been reported that the change of V_{th} was proportional to the density of the charges in dielectric layer.[42] Thus, the large V_{th} shift in the positive direction strongly suggests the increase of stored charges with enhancing the PCBM composition. The above effect can be attributed to the transfer of charge carrier from semiconductor into the dielectric, which is controlled by the applied gate voltage and known as a tunneling process.

To analyze such charge transfer, we herein propose the possible mechanism of BPE-PTCDI-based transistor memory using the energy-band diagram (Figure 4a). During the writing process, a negative gate bias would induce the positive charge carrier at the semiconductor–dielectric interface and reduce the HOMO energy barrier between BPE-PTCDI and N-(PTPMA)$_3$. Simultaneously, the induced positive charge carriers are injected into the dielectric (Figure 4b). Due to the built-in electric field induced from these stored charges, the negative mobile carriers in the channel can easily accumulate at the interface, resulting in the much more negative shift in the transfer plot. Therefore, the high conductive state of the device is retained even when the gate bias is removed. As a positive gate bias is applied (the erasing process), the negative carriers can pass through the N(PTPMA)$_3$ matrix and reach the LUMO level of the PCBM (−3.7 eV) to first neutralize the irreversible charges stored in the HOMO level of N(PTPMA)$_3$ and subsequently trap electrons in PCBM.[43] As a result, the memory device can return to the initial state or even create a positive-shift erasing curve depending on the composition of

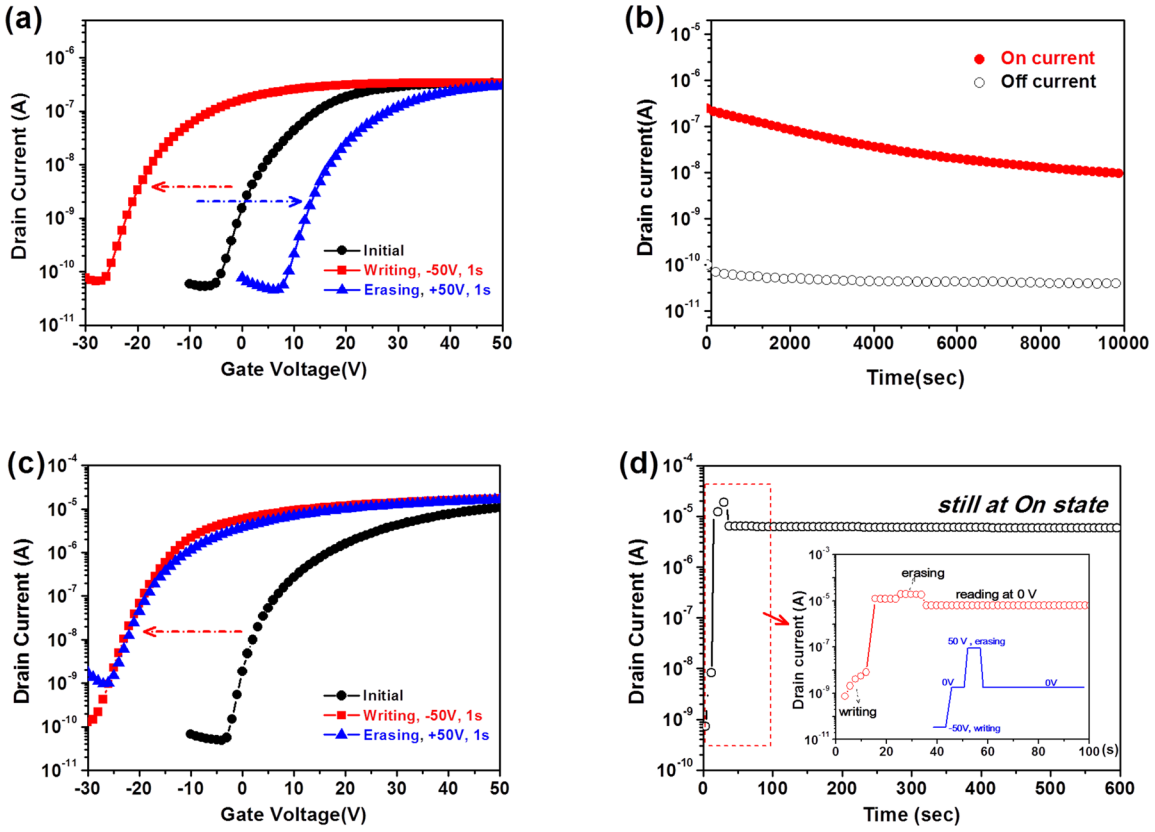

Figure 8. Transfer curves of transistor memory devices using different electrets: (a) 5 wt % TIPS-pen:N(PTPMA)$_3$ and (c) 5 wt % ferrocene:N(PTPMA)$_3$ dielectric for control experiment. (b) Retention characteristics of BPE-PTCDI-based OFET memory devices with 5 wt % TIPS-pen:N(PTPMA)$_3$ dielectrics measured at a gate voltage of 0 V and drain-source voltage of 30 V. (d) Switching behavior of device of 5 wt % ferrocene:N(PTPMA)$_3$ dielectric.

PCBM. Its memory behavior switches repeatedly, and the device becomes a nonvolatile flash memory.

In addition, the hysteresis window, the term of distinction of V_{th} shift between the forward and backward switching, is one of the indicative information on the memory effect. The high and low conductance within the fixed gate scanning range upon the dual-sweeping is summarized in Figure 5. The hysteresis loop denotes a net electron trapping effect,[34,35,37,43] and the memory ratio, defined as the drain current ratio at a fixed gate voltage between forward and backward switching,[44] is apparently related to the channel resistance modulated by the PCBM composition. Without adding the PCBM in the electret, the device shows a weak hysteresis with a relatively small memory ratio of 3.58. When PCBM is blended, the devices show bistable states with the memory ratio increased to 348.86 at 1 wt % PCBM and larger than 10^3 at 3 wt % or higher PCBM. Besides, the hysteresis window is more than half of the total sweep-voltage range. Such prominent hysteresis shows the high operation speed for the high performance of memory devices.[33] However, the hole trapping ability of the device using the 5 wt %PCBM:N(PTPMA)$_3$ electret is slightly unstable compared to its parent N(PTPMA)$_3$ matrix according to the shift of the writing curve (i.e., reflecting a relatively larger standard deviation on V_{th} of the writing process). Although the charge capacity gradually enlarges as the critical content of PCBM increases, the high-conductance in the 5 wt % PCBM:N-(PTPMA)$_3$ electret is likely induced by the distinct aggregation of PCBM, thus leading to the charge dissipation.

To make the nonvolatile capacity of the memory device clear, the retention characteristics of the BPE-PTCDI transistor memories using the PCBM:N(PTPMA)$_3$ electret are studied. As shown in Figure 6, after the writing/erasing process, the reading state is read at the gate-source voltage of 0 V. Initially, the ON/OFF current ratio is larger than 10^3, although the ON current is then decayed rapidly in the front period of 1500 s. The charge reveals until the equilibrium reaches. The high and low conducting state can keep longer than 10^4 s for the three studied devices. The stable stored data retention suggests a promising feature for nonvolatile memory devices. Furthermore, the cyclic switching test on the transistor memories using the blend electret is studied to endure long-term dynamic switching. The cyclic duration is measured at the drain-source voltage of 30 V and under the gate voltages of +50, 0, and −50 V for the processes of writing, reading, and erasing, respectively. As shown in Figure S6 (Supporting Information), the device using the 50 nm thick 5 wt % PCBM:N(PTPMA)$_3$ electret is gradually destroyed after a few cycles of repeating measurements. There are several spots with a diameter of about 20 μm left on the drain electrode, suggesting the rupture of the dielectric layer due to the charge and heat accumulation after continuously cyclic switching operations.[45,46] The extent of the rupture has been reported to be inversely proportional to the thickness of the dielectric. Therefore, the modification of dielectric thickness is resistant to the above catastrophic rupture. To enhance the long-term stability of the device, a layer of high-k hydrophilic poly(methacrylic acid) (PMAA, ca. 100 nm thickness)[36] was inserted beneath the chargeable

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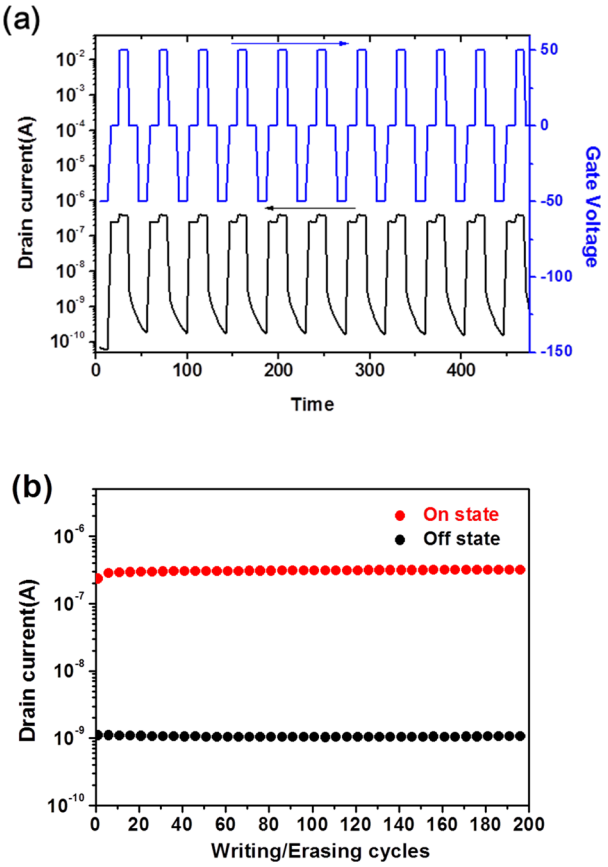

Figure 9. (a) Switching behavior for BPE-PTCDI-based memory device with modified 5 wt % TIPS-pen:N(PTPMA)$_3$ dielectric film, and (b) the record of ON and OFF current of 200 cycles for the switching behavior.

PCBM:N(PTPMA)$_3$ electret to form a bilayer polymer dielectric. As shown in Figure 7a,b, the bilayer polymer dielectric shows the similar memory behavior with that of blended compositions as reported in the literature.[21] The hydrophilic PMAA is used as the bottom layer to enhance the thickness as well as reduce the impact of electric field for the long-term operation. As a result, the device using a bilayer of 5 wt %PCBM:N(PTPMA)$_3$ and PMAA can switch reversibly up to 140 cycles (Figure 7c,d).

3.2. Effect of the Donor:N(PTPMA)$_3$ Electret on Memory Characteristics. The effect of semiconducting materials used as the trap in the matrix on the charge transfer has been investigated because they have been reported to significantly affect charge transfer.[33,47] In this work, TIPS-pen (−3.11 eV)[48] and ferrocene (−1.91 eV)[33] with high LUMO levels are used and blended with N(PTPMA)$_3$. Note that TIPS-pen and ferrocene have a stronger electron-donating ability than BPE-PTCDI and PCBM. The charge-transfer characteristics of various thin-film transistor (TFT) memories are shown in Figure 8 and Table 1. Similar to the results of the device using the 5 wt % PCBM:N(PTPMA)$_3$ electret, the devices using the N(PTPMA)$_3$:TIPS-pen electret reveal a flash-type characteristic (Figure 8a) because of the slightly higher LUMO barrier (1.10 eV) between BPE-PTCDI and TIPS-pen than that of the PCBM case (0.51 eV). It enables the electric-field-induced electrons to tunnel through the N(PTPMA)$_3$ into the TIPS-pen and the transfer curve has the positive shift (~11 V) as applying positive bias, which leads a erasable transfer curve and bistable ON/OFF retention stability over 10^4 s (Figure 8b). However, the electron-trapping capabilities of 5% TIPS-pen and 5% PCBM are close even though the energy barrier difference is 0.5 eV between them, which is probably due to the aggregated morphologies. From the TEM image (Figure S1c, Supporting Information), the 5 wt % PCBM:N(PTPMA)$_3$ film with ca. 20 nm aggregates of PCBM could limit the shift of threshold voltage after a writing operation. On the contrary, the 5 wt % TIPS-pen:N(PTPMA)$_3$ thin film shows a well-dispersed morphology in Figure S1d (Supporting Information) because the triisopropylsilylethynyl groups in TIPS-pen are miscible with N(PTPMA)$_3$ in toluene solution. Therefore, the electron trapping abilities contributed by PCBM and TIPS-pen are similar.

On the other hand, the OTFT memory using the N(PTPMA)$_3$:ferrocene electret, interestingly, shows an irreversible behavior once it switches to the ON state (Figure 8c) and no hysteresis showed upon dual-sweeping (Figure S7, Supporting Information). Furthermore, the memory property under continuous writing-reading-erasing-reading operations is shown in Figure 8d, in which the read current maintains at the ON state for a period of the retention time even after exerting the pulses of erasing voltage. This fact indicates the device using the N(PTPMA)$_3$:ferrocene electret possesses the WORM-type memory property. The transform of memory behavior can be attributed to the larger gap of the LUMO energy level (2.3 eV) between BPE-PTCDI and ferrocene than those between BPE-PTCDI and TIPS-pen (1.1 eV) or PCBM (0.51 eV).

When the charge-transfer behaviors of different devices are compared using the PCBM:N(PTPMA)$_3$, TIPS-pen:N(PTPMA)$_3$, and ferrocene:N(PTPMA)$_3$ electrets, the obvious charge injection in the writing process can be considered to correlate with the higher HOMO level of N(PTPMA)$_3$ (−5.48 eV) than that of BPE-PTCDI (−6.02 eV), which would effectively stabilize the positive carriers. It is likely that no significantly enhanced writing effect is observed using the electron-donating materials with a higher HOMO level, such as TIPS-pen (−5.0 eV)[48] or ferrocene (−4.8 eV),[33] perhaps because the strong hole-stability nature of the N(PTPMA)$_3$ matrix dominates the hole-trapping behavior. Also, the hysteresis phenomena of the writing curves exhibit the dual-sweeping with the high electron affinity (Figure S7, Supporting Information), similar to the trend of the memory window. Moreover, after the thickness modification by inserting a PMAA layer into the dielectric, the memory devices using the TIPS-pen:N(PTPMA)$_3$ electret behave as flash-type memories and can perform the erasing or writing operations continuously up to 200 cycles (Figure 9). It indicates that the organic materials with different electron affinities can significantly tune the FET memory characteristics.

4. CONCLUSIONS

We employed the BPE-PTCDI-based nonvolatile transistor memory devices using blends of a semiconducting molecule and N(PTPMA)$_3$ as the gate dielectric. The memory characteristic changed from irreversible (WORM) to reversible (flash) after blending PCBM into the N(PTPMA)$_3$ layer and the memory window was enhanced from 0.26 to 30.96 V as the PCBM content was increased from 0 to 5 wt %. The energy level of the semiconducting moiety showed a significant effect on the memory characteristics. As the ferrocence with a higher LUMO level blended into the N(PTPMA)$_3$ dielectric, the flash-type memory changed to the WORM-type memory. All the

studied memory devices exhibit a long retention over 10^4 s with a highly stable read-out current. Also, they could have the repeat cycles of write-read-erase-read (WRER) as many as 200 times using the bilayer electret structure of inserting poly(methacrylic acid). Our result suggested that the energy level and charge transfer in the semiconducting blend electret could tune the characteristics of nonvolatile transistor memory devices.

■ ASSOCIATED CONTENT

Supporting Information

TEM and AFM images of polymer electrets, transfer curves of the transistor devices without polymer electrets, the overlapped curves for the writing and erasing processes of PCBM:$N(PTPMA)_3$, the switching behavior of $N(PTPMA)_3$, switching behavior for BPE-PTCDI-based memory device with 5% PCBM:$N(PTPMA)_3$, the optical image before cyclic switching test and after the test, and hysteresis loop of BPE-PTCDI-based TFT memory with various polymer blends operated in the writing process. This material is available free of charge via the Internet at http://pubs.acs.org.

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Notes

The authors declare no competing financial interest.

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